

### **REMARKS**

The present Amendment amends claims 21, 23, 24 and 26 and adds new claims 27-42. Therefore, the present application has pending claims 21, 23, 24 and 26-42.

The title of the invention stands objected to as not being descriptive. The title of the invention as changed to "STORAGE SYSTEM HAVING DATA FORMAT CONVERSION FUNCTION" which Applicants submit is descriptive of the present invention. Therefore, this objection is overcome and should be withdrawn.

Claim 23 stands objected to due to an informality noted by the Examiner in paragraph 2 of the Office Action. Amendments were made to claim 23 to correct the informality noted by the Examiner, particularly with regard to the dependency of claim 23. Therefore, this objection is overcome and should be withdrawn.

Claims 21, 23, 24 and 26 stand rejected under 35 USC §102(e) as being anticipated by Hashemi (U.S. Patent No. 5,337,414). This rejection is traversed for the following reasons. Applicants submit that the features of the present invention as now recited in claims 21, 23, 24 and 26 are not taught or suggested by Hashemi whether taken individually or in combination with any of the other references of record. Therefore, Applicants respectfully request the Examiner to reconsider and withdraw this rejection.

Amendments were made to each of claims 21, 23, 24 and 26 so as to more clearly recite that the present invention is directed to a storage system having a plurality of host adaptors coupled to at least one host device which form interfaces for the host device, a plurality of storage devices for storing therein data transferred

from the host device, a plurality of disk adaptors coupled to the storage devices, at least one cache for temporarily storing therein data transferred between the host adaptors and the disk adaptors, two buses coupled to the host adaptors, the disk adaptors and the cache which transfer data among the host adaptors, disk adaptors and cache, wherein the two buses operate as a pair of buses having a transfer ability larger than that of the two buses, a memory for storing a status of which of the two buses is available for use due to a failure in other of the two buses, and a format converter for converting a format of data sent from the host device into a second format suitable for the storage devices and sending the converted data of the second format to the cache through the two buses.

Thus, as clear from the above, the storage system according to the present invention as illustrated in Figs. 2 and 3 includes a data format converter (7) for converting the format of data sent from the host device into the format suitable for the storage devices (5). The data format converter (7) sends the data, the format of which has been converted to the format suitable for the storage devices, to the buses. The cache memory unit (3) stores therein the converted data thus sent through the bus.

According to the above described configuration of the present invention, even in the case where the data format of the host device and the data format of the storage devices differs, information communication can be performed between the host device and the storage devices by use of the data format converter (7). According to the present invention, since the data format conversion is performed at the data format converter (7) of the host adaptors (first logical units) provided

between the host device and the cache memory unit (3), the cache memory can store data of the same format as that used for the storage devices. As a result, according to the present invention information can be transmitted at a high speed between the cache memory and the storage devices.

Further according to the present invention, even when the host adapters (first logical units) are coupled to the host devices having different data formats, the host devices can commonly share the storage devices due to the independent data format conversion performed in each of the host adaptors. According to the present invention, since data of a single or same data format is stored in the cache memory unit, information can be transmitted at a high speed between the host adaptor and the storage devices.

The above described features of the present invention are not taught or suggested by any of the references of record whether taken individually or in combination with each other. Particularly, the above described features of the present invention are not taught or suggested by Hashemi.

Hashemi teaches a mass data storage/retrieval module for controlling the storage and retrieval operations of massive amount of data in disk storages. As taught by Hashemi, a buffer memory system is provided in each of the interface control modules so as to permit simultaneous and concurrent writing to buffer storage and reading out of data from the buffer storage through multiple ports.

At no point is there any teaching or suggestion in Hashemi of a format converter which converts a first format of data from a host device into a second format suitable for storage on the disk storage device and the storing of the

converted data in the second format in a cache prior to storing on the disk storage device as in the present invention. As described above, Hashemi merely teaches the use of a buffer memory system for temporarily storing data prior to the data being stored on the disk storage devices. Hashemi simply teaches the use of multiple ports which can be operated independently from each other.

Thus, Hashemi fails to teach or suggest a format converter for converting a first format of data sent from the host device into a second format suitable for the storage devices and sending converted data of the second format to the cache through the two buses of the storage system as recited in the claims.

Therefore, Applicants respectfully request that the Examiner reconsider and withdraw the above described rejection of claims 21, 23, 24 and 26 under 35 USC §102(e) as being anticipated by Hashemi.

As indicated above, the present Amendment adds new claims 27-42. New claims 27-42 recite many of the same features shown above not to be taught or suggested by Hashemi. Therefore, the same arguments presented above distinguishing the features of the present invention as recited in claims 21, 23, 24 and 26 with respect to Hashemi apply as well to the potential use of Hashemi to reject claims 27-42.

Claims 21 and 24 stand rejected under the judicially created doctrine of obviousness type double patenting as being unpatentable over claims 1 and 2 of prior Patent No. 6,581,128. This rejection is traversed for the following reasons. Applicants submit that the features of the present invention as now recited in claims 21 and 24 are not taught or suggested by claims 1 and 2 of the prior patent nor do

they improperly extend the right to exclude already granted in the prior patent.

Therefore, reconsideration and withdrawal of this rejection is respectfully requested.

As indicated above, amendments were made to claims 21 and 24 to more clearly recite that the present invention provides a storage system including a format converter for converting a first format of data sent from the host device into a second format suitable for the storage devices and sending converted data of the second format to the cache through the two buses. These features now recited in claims 21 and 24 are not taught or suggested by claims 1 and 2 of the prior patent.

Claims 1 and 2 of the prior patent are each directed to a storage system wherein a memory is provided for storing management information including degraded operation information in a management area of the memory and wherein the degraded operation information indicates which of the two buses is available for use due to a failure in the other of the two buses. As taught in each of claims 1 and 2 of the prior patent, the degraded operation information stored in the memory can be referred to by an external processor and when a first bus of the two buses is in a degraded state as indicated by the degraded operation information then a second bus is used for transferring management information.

As is quite clear from the above, the features recited in claims 1 and 2 of the prior patent do not teach or suggest the format converter described above now recited in claims 21 and 24. Each of claims 1 and 2 of the prior patent are simply directed to a storage which makes use of degraded operation information so as to account for degraded operation of the storage system, whereas each of claims 21 and 24 of the present application are directed to providing a format converter so as

to permit the conversion of the format of data sent from a host device to a single format suitable for the storage devices so as to permit its high speed transmission on the buses to a cache suitable and ultimately to the storage devices.

Thus, claims 21 and 24 do not improperly extend the right to exclude already granted in the prior patent since the invention now recited in claims 21 and 24 are not covered by each of claims 1 and 2 of the prior patent. Therefore, reconsideration and withdrawal of the judicially created doctrine of double patenting rejection of claims 21 and 24 as being unpatentable over claims 1 and 2 of the prior patent is respectfully requested.

The remaining references of record have been studied. Applicants submit that they do not supply any of the deficiencies noted above with respect to the reference utilized in the rejection of claims 21, 23, 24 and 26.

In view of the foregoing amendments and remarks, Applicants submit that claims 21, 23, 24 and 26-42 are in condition for allowance. Accordingly, early allowance of claims 21, 23, 24 and 26-42 is respectfully requested.

To the extent necessary, the applicants petition for an extension of time under 37 CFR 1.136. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, or credit any overpayment of fees, to the deposit account of Antonelli, Terry, Stout & Kraus, LLP, Deposit Account No. 01-2135 (500.33021CX5).

Respectfully submitted,

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